# 7nm Custom / MS Reference Flow

## Cadence

# ABSTRACT

7nm FinFET technology offers great advantages in power and area reduction for digital designs, but escalating challenges in scaling custom circuits due to increased impact of device parasitics and discrete device dimensions and more complex and restrictive design, electro-migration and reliability rules. To address these challenges custom designers need highly automated layout flow supported by advanced analysis through layout design and signoff.

The presentation will cover integrated flow developed in collaboration among TSMC and Cadence. The flow is modular and includes among others:

- Variability analysis in Virtuoso ADE utilizing TSMC's Variability-aware API for more efficient statistical sampling

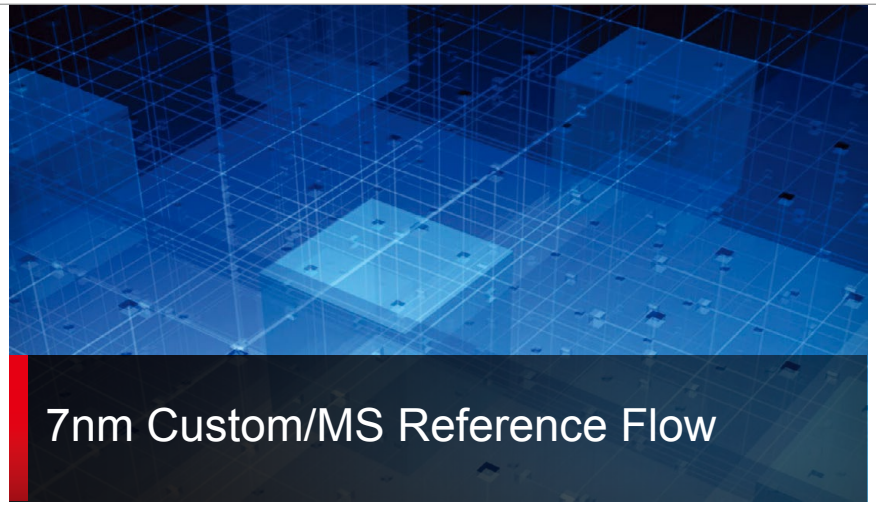
- Device placement utilizing Virtuoso constraint and LDE-aware and TSMC Array-API capabilities for more productive layout

- Due to increased device complexity and its parasitics a new innovative method is required to better predict design performance in pre-layout stage and ensure correlation with post-layout simulation results. Virtuoso capabilities as well as TSMC provided Macro-device approach, minimally disturbing existing schematic driven use model will be presented.

- Color-aware and electrically-aware routing

- Signal and power Electro Migration and IR Drop at design and Signoff levels with impacts of device self-heating.

The results of flow validation on VCO design will be presented.



# 7nm Custom/MS Reference Flow

Jim McMahon, Product Engineering Director, Cadence
TSMC OIP Ecosystem Forum
San Jose, CA
September 22, 2016

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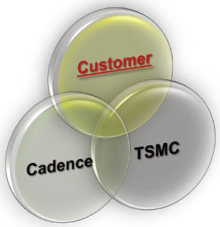
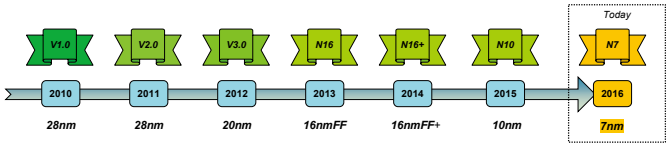
## TSMC-Cadence Collaboration

### Mixed-signal methodologies, reference flows, and enablement

- Provide methodologies for robust designs, better quality of results and higher yield
- Improve design productivity with automation, correct-by-construction, and reuse
- Accelerate adoption of new technology and methodology by common customers



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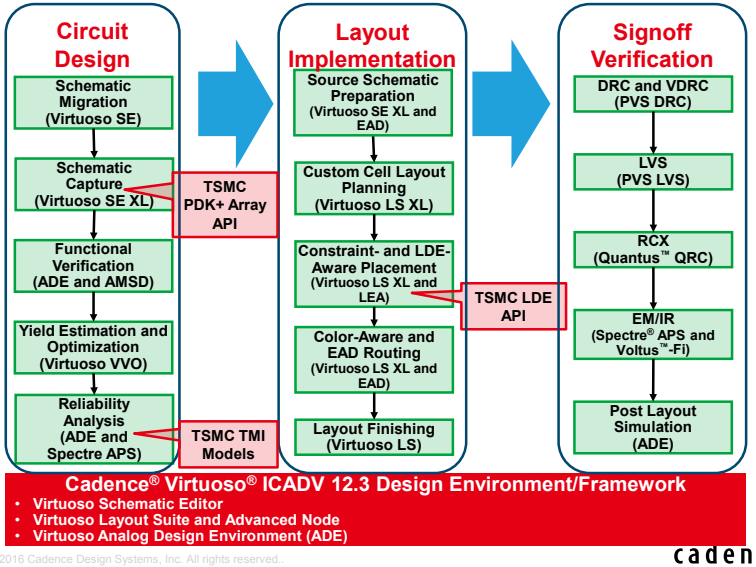
## 7nm Custom Design Reference Flow (CDRF) Modules



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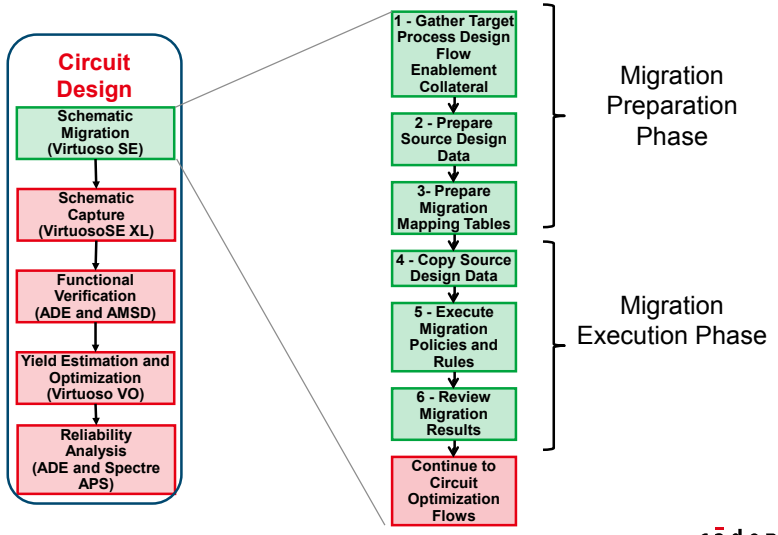
## Custom Circuit Design Flow Modules

### Sub-module: Schematic migration



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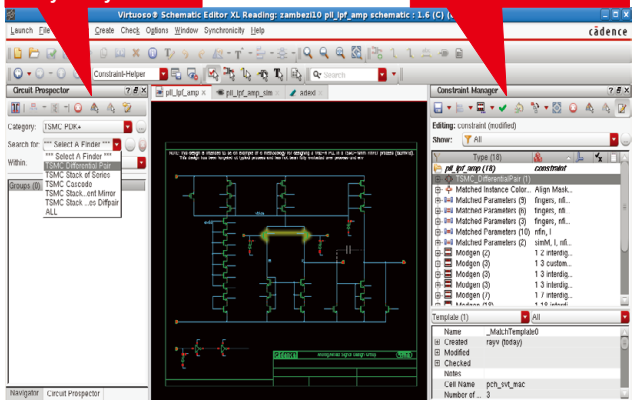
# Custom Circuit Design Flow Modules

## Sub-module: Schematic capture

**Circuit Design**
- Schematic Migration (Virtuoso SE)
- Schematic Capture (Virtuoso SE XL)
- Functional Verification (ADE and AMSD)
- Yield Estimation and Optimization (Virtuoso VO)
- Reliability Analysis (ADE and Spectre APS)



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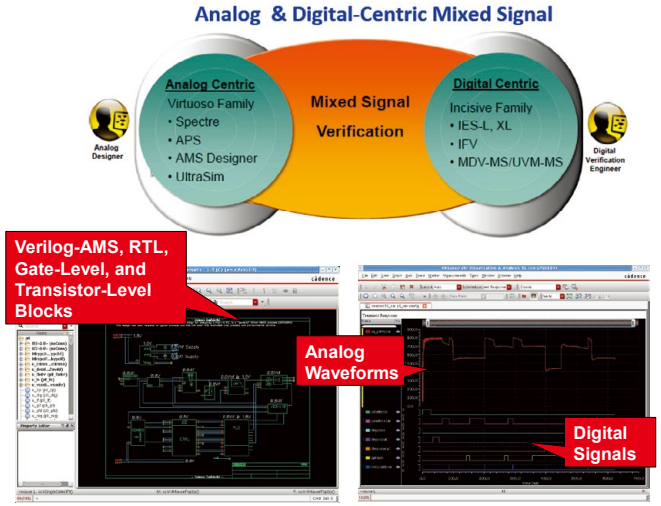
# Custom Circuit Design Flow Modules

## Sub-module: Mixed-signal functional verification

**Circuit Design**
- Schematic Migration (Virtuoso SE)
- Schematic Capture (Virtuoso SE XL)
- Functional Verification (ADE and AMSD)
- Yield Estimation and Optimization (Virtuoso VO)
- Reliability Analysis (ADE and Spectre APS)




Cadence Incisive® Family:
- Incisive Enterprise Simulator L and XL
- Incisive Formal Verifier
- Metric-driven verification for mixed signal (MDV) and Universal verification methodology for mixed-signal (UVM-MS)

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# Custom Circuit Design Flow Modules

## Sub-module: Yield optimization and verification

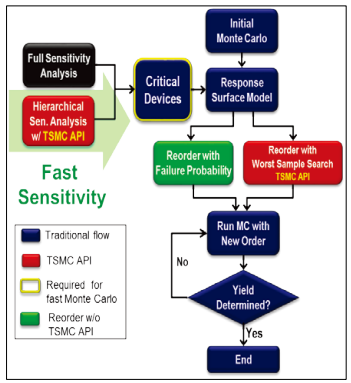
**Circuit Design**
- Schematic Migration (Virtuoso SE)
- Schematic Capture (Virtuoso SE XL)
- Functional Verification (ADE and AMSD)
- Yield Estimation and Optimization (Virtuoso VO + Spectre APS)
- Reliability Analysis (ADE and Spectre APS)

Conventional Flow
(without sample reduction)
- Vth sensitivity analysis
- Monte Carlo simulation

Advanced Flow
(with sample reduction)
- Vth sensitivity analysis
- Monte Carlo simulation

High-Sigma Monte Carlo [PDK+] Use Variation-API
- Vth sensitivity analysis for simulation reduction
- Sample reorder Monte Carlo for sample reduction

***Virtuoso VO + TSMC API Fast Monte Carlo Flow***



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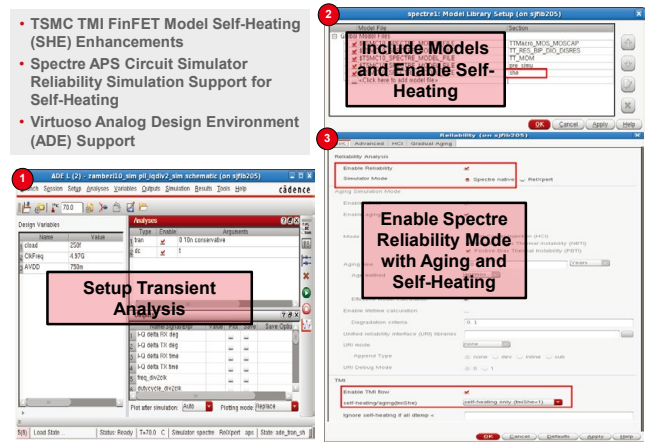
# Custom Circuit Design Flow Modules

## Sub-module: Reliability analysis

**Circuit Design**
- Schematic Migration (Virtuoso SE)
- Schematic Capture (Virtuoso SE XL)
- Functional Verification (ADE and AMSD)
- Yield Estimation and Optimization (Virtuoso VO + Spectre APS)
- Reliability Analysis (ADE and Spectre APS)

- TSMC TMI FinFET Model Self-Heating (SHE) Enhancements
- Spectre APS Circuit Simulator Reliability Simulation Support for Self-Heating
- Virtuoso Analog Design Environment (ADE) Support



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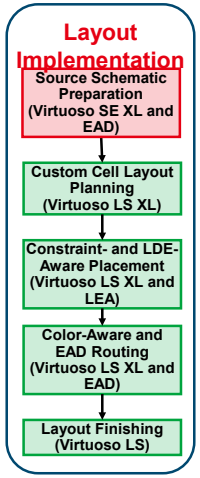
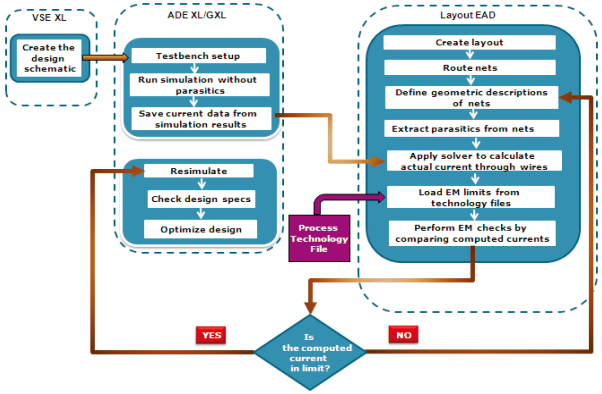
# Custom Layout Implementation Flow Modules

## Sub-module: Source schematic preparation




***Virtuoso ADE + Electrically Aware Design (EAD) Flow Overview***



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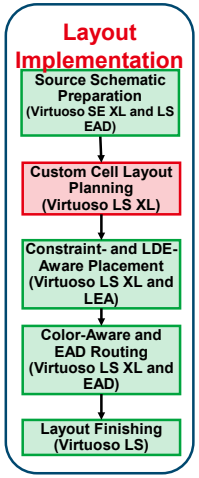
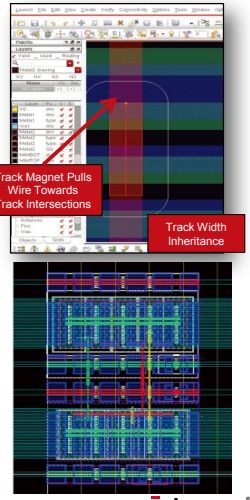
# Custom Layout Implementation Flow Modules

## Sub-module: Cell layout planning

Row-Based Placement and Track-Based Routing Setup




- Width spacing patterns (WSPs)
  - Sophisticated "correct by construction" non-uniform routing grid with pre-defined width and color constraints
  - Novel methodology that aids in productivity and reduces design complexity
- Coloring using WSPs
  - When WSPs are defined with colors, OA objects inherit colors of tracks used to create and edit wires
  - Pin creation
    - Pins snap to tracks
  - New wire editor enhancements
    - Wires snap to tracks
    - Track magnet pulls the wire towards track intersection
    - Wire inherits track widths
    - Improved dynamic display of tracks on upper and lower layers
    - Auto via insertion



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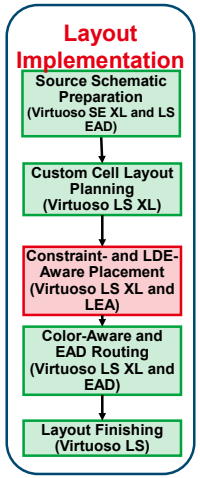
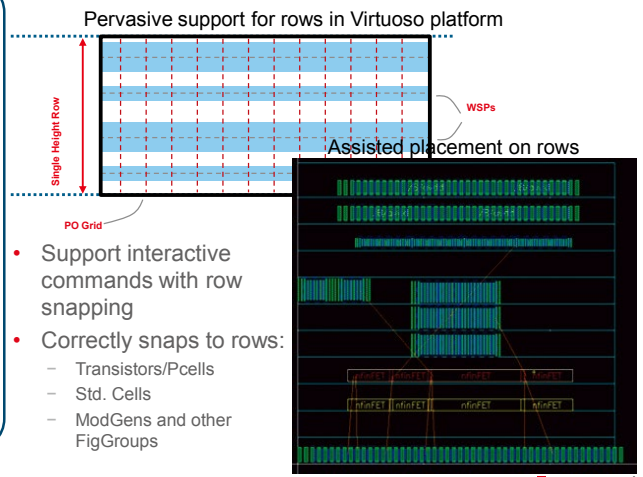
# Custom Layout Implementation Flow Modules

## Sub-module: Constraint- and LDE-aware placement




- New unified placement flow and advanced-node row-based placement technology




- Support interactive commands with row snapping
- Correctly snaps to rows:
  - Transistors/Pcells
  - Std. Cells
  - ModGens and other FigGroups

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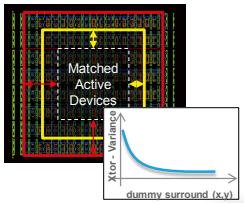
# Custom Layout Implementation Flow Modules

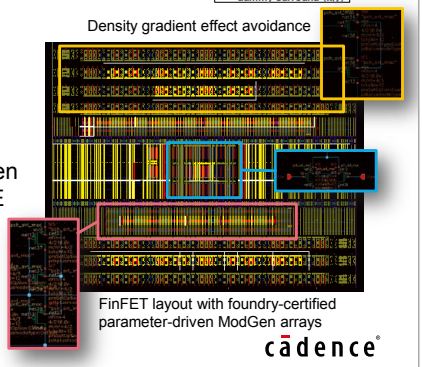
## Sub-module: Constraint- and LDE-aware placement

Density gradient effects (DGEs) avoidance using ModGens

- Structured place and route environment of ModGens is ideal for automatically building highly matched layout blocks
- Support for array-based entry, identical dummy insertion, and complex guard ring creation instrumental in avoiding DGEs
- Streamlined dummy back annotation enables LVS clean schematics
- Rich library of TSMC co-developed ModGen constraint templates further automate DGE clean layout construction




Density gradient effect avoidance



FinFET layout with foundry-certified parameter-driven ModGen arrays

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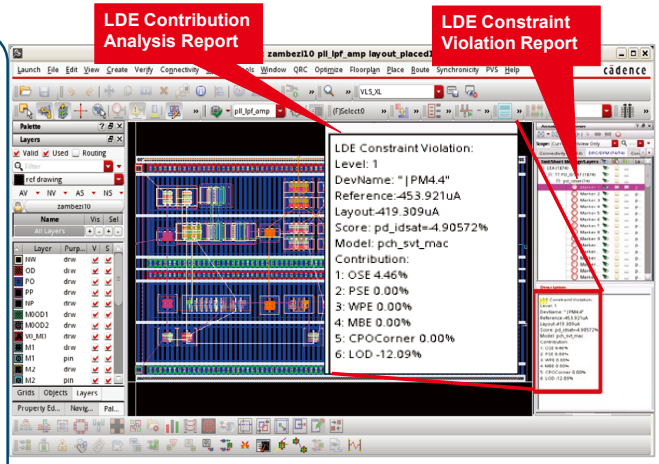
# Custom Layout Implementation Flow Modules

## Sub-module: Constraint- and LDE-aware placement

**Layout Implementation**

- Source Schematic Preparation (Virtuoso SE XL and EAD)
- Custom Cell Layout Planning (Virtuoso LS XL)
- Constraint- and LDE-Aware Placement (Virtuoso LS XL and LEA)
- Color-Aware and EAD Routing (Virtuoso LS XL and EAD)
- Layout Finishing (VirtuosoLS)



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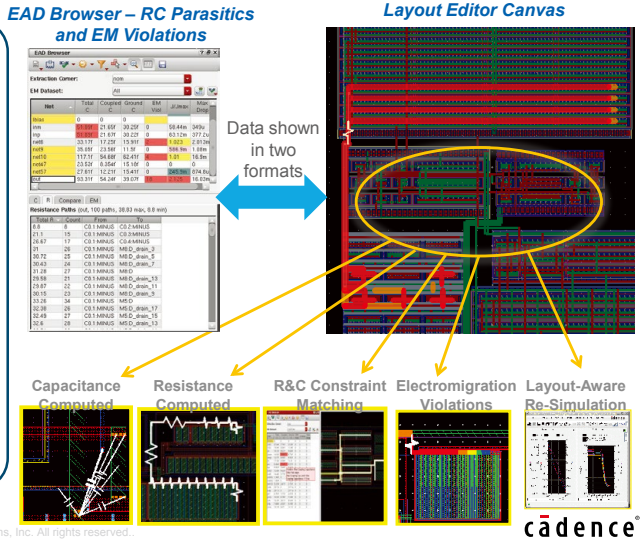
# Custom Layout Implementation Flow Modules

## Sub-module: Color-aware and EAD routing

**Layout Implementation**

- Source Schematic Preparation (Virtuoso SE XL and LS EAD)
- Custom Cell Layout Planning (Virtuoso LS XL)
- Constraint- and LDE-Aware Placement (Virtuoso LS XL and LEA)
- Color-Aware and EAD Routing (Virtuoso LS XL and EAD)
- Layout Finishing (Virtuoso LS)



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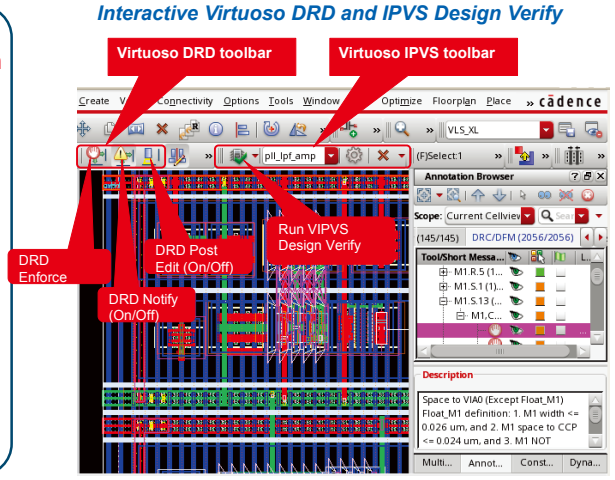
# Custom Layout Implementation Flow Modules

## Sub-module: Color-aware and EAD routing

**Layout Implementation**

- Source Schematic Preparation (Virtuoso SE XL and LS EAD)
- Custom Cell Layout Planning (Virtuoso LS XL)
- Constraint- and LDE-Aware Placement (Virtuoso LS XL and LEA)
- Color-Aware and EAD Routing (Virtuoso LS XL and EAD)
- Layout Finishing (Virtuoso LS)



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# Custom Layout Implementation Flow Modules

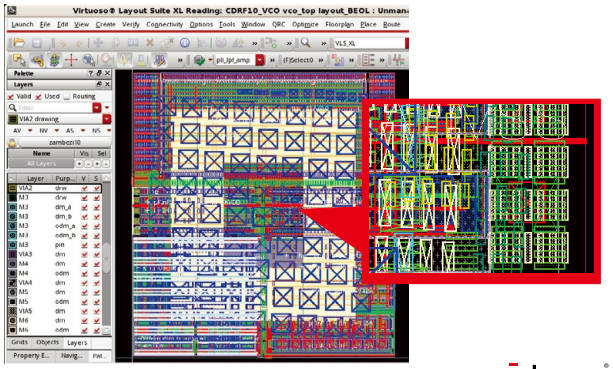
## Sub-module: Layout finishing

**Layout Implementation**

- Source Schematic Preparation (VSE XL and EAD)
- Custom Cell Layout Planning (VLS XL)
- Constraint- and LDE-Aware Placement (VLS XL and LEA)
- Color-Aware and EAD Routing (VLS XL and EAD)
- Layout Finishing (VLS)

Final layout with FEOL and BEOL patterns

- Generate FEOL and BEOL patterns via PVS-DRC utility
- Import the generated patterns (GDS) into Virtuoso (OA) platform
- Overlay the pattern views onto the *layout* view





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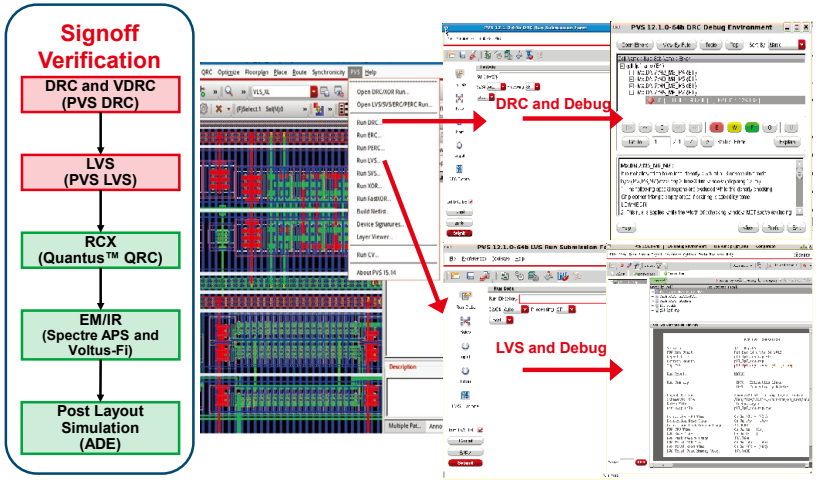
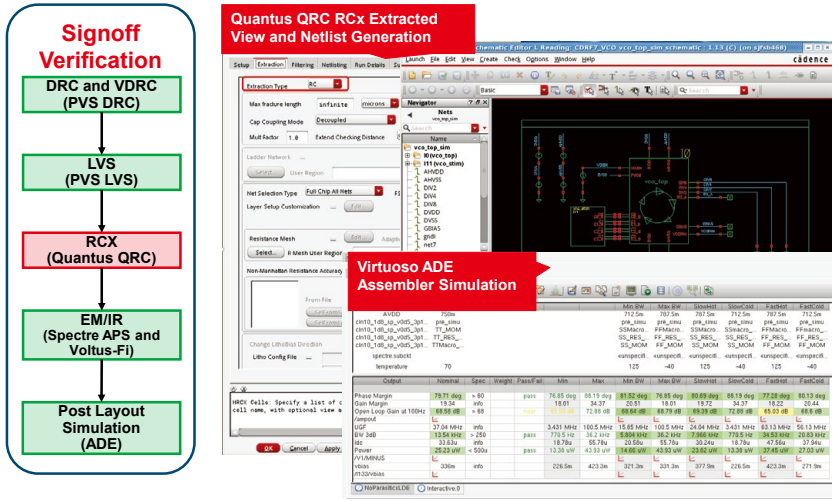
## Custom Layout Implementation Flow Modules
### Sub-module: Signoff flow—DRC and LVS



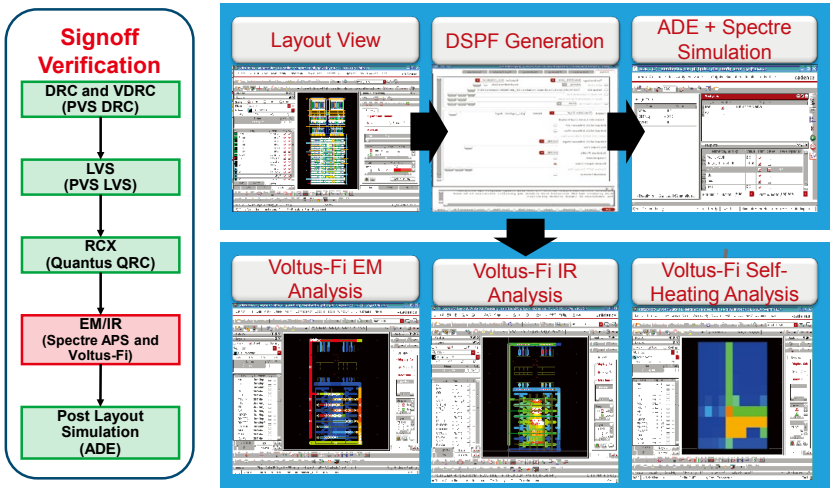



## Custom Layout Implementation Flow Modules
### Sub-module: Signoff flow—RCx extraction



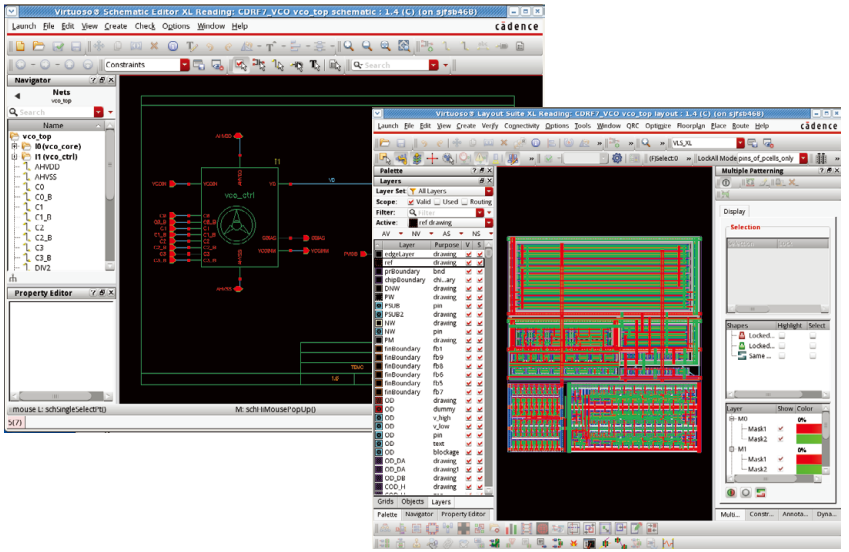



## Custom Layout Implementation Flow Modules
### Sub-module: Signoff flow—RCx extraction






## Final Schematic and Layout



## Summary

- TSMC and Cadence continue close collaboration on addressing custom and mixed-signal design challenges at advanced-process nodes
- Custom flow for N7 FinFET technology is another milestone containing key enhancements required for faster adoption by common customers
- The flow offers advanced methodology and unique features for productivity improvements, electrical analysis for better predictability and design closure, and higher quality of silicon

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